UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,421	03/25/2004	Masafumi Takahashi	251020US2	5331

22850 7590 06/26/2006

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,421	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 are present for examination.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (03/26/203) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings are accepted since there appear to be no issues regarding the drawings filed with the application on 03/25/2004.

Claim Objections

Claim 1 is objected to because of the following informalities:

There is a grammatical error in line 7 of the claim.

Appropriate correction is required. Examiner recommends replacing "connected one another" in line 7 of the claim with "connected to one another" to overcome this objection.

Claim 5 is objected to because of the following informalities:

There is improper punctuation at the end of line 8 of the claim.

Appropriate correction is required. Examiner recommends replacing the "," at the end of line 8 of the claim with "; and" to overcome this objection.

Claim 7 is objected to because of the following informalities:

There is a grammatical error in line 9 of the claim.

Appropriate correction is required. Examiner recommends replacing "in a halt" at in line 9 of the claim with "to a halt" to overcome this objection

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6 it is unclear to the examiner how a serial-to-parallel converter is used when there are three inputs supplied to the converter wherein only one of those inputs is converted into parallel data wherein there is only a single output from the converter indicating that it is really a parallel-to-serial converter. For the purposes of this examination examiner will treat the "serial-to-parallel converter" as being a parallel-to-serial converter such as the one illustrated in figures 5, 4, and 3 of this applications such as one of ordinary skill in the art would understand it to be. Appropriate corrections and or explanations is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA) as evidenced by Rajski et al. (US 6728901), Johnson (4811345), Sagawa et al. (3872245), patent number 3623020, and Nagel et al. (4188665).

1. As per claim 1, AAPA teaches A logic circuit having a self-test function comprising:

A plurality of scanning flip-flops (F/F) circuits having at least a first-stage scanning F/F circuit, a second-stage scanning F/F circuit and a last-stage scanning F/F circuit, each having a clock input terminal, a scanning input terminal and a scanning output terminal, the scanning F/F circuits being connected one another so that a scanning clock signal is input to the clock input terminal of each

scanning F/F circuit and a signal output from the scanning output terminal of the first-stage scanning F/F circuit is supplied to the scanning input terminal of the second-stage scanning F/F circuit for sequential logical operations (figure 6 with pages 1-2 lines 33-33);

AAPA does not specifically teach:

The plurality of scanning F/F with a feed-back signal line connecting the output of the last-stage scanning F/F to the input of the first-stage scanning F/F;

At least one data selector selecting either an external scanning signal or the signal fed back form the last-stage scanning F/F to be supplied to the input terminal of the first-stage scanning F/F;

At least one scanning controller supplying a control signal to the data selector to select which signal supplied to the data selector is supplied to the input terminal of the first-stage F/F; and

An external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit.

However those of ordinary skill in the art at the time the invention was made would recognize that a liner feedback shift register (LFSR) is well known. The art is replete with references; see for example within the attached 892 figure 12 and column 12 in Rajski et al. (US 6728901) wherein a LFSR is disclosed.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to create a LFRS such as the one taught by Rajski with

AAPA multiple stage scanning F/F circuit in order to expand compressed data with minimum components.

2. As per claim 2, AAPA as modified teaches wherein the scanning controller supplies the control signal to the data selector based on a processor instruction of a prestored program. Examiner notes that a scanning controller supplying a control signal to the data selector based on a processor instruction is required for selection of either the feedback signal or input data as the input to the first-stage F/F. The art is replete with references; see for example within the attached 892 figure 12 in Rajski et al. (US 6728901) wherein a control signal is required to select between SEED and the feedback of the LFSR (206).

3. As per claim 3, AAPA as modified teaches wherein the scanning controller supplies the control signal to the data selector based on a processor instruction of a prestored program.

AAPA as modified does not specifically teach wherein the processor instruction is a reduced instruction set computer (RISC) instruction.

However those of ordinary skill in the art at the time the invention was made would recognize that the processor instructions being a reduced instruction set computer (RISC) instructions is well known. The art is replete with references; see for example within the attached 892 columns 1-2 lines 64-7 in Johnson (4811345) wherein RISC is disclosed.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to have the processor instructions within AAPA as modified

be RISC instructions since by doing so it would reduce complexity of the system since as stated by Johnson RISC architecture is a simplified instruction set that can provide sequencing control signals easily to a processor (Johnson - column 1-2 lines 64-7).

4. As per claim 4, AAPA as modified teaches wherein the scanning controller supplies the control signal to the data selector based on a processor instruction of a prestored program.

AAPA as modified does not specifically teach wherein there further comprises:

At least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit; and

An external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output from the logic circuit.

However those of ordinary skill in the art at the time the invention was made would recognize that a selector for selecting between an external or internal clock being supplied to the clock input terminal of each scanning F/F along with an external clock output terminal via which the selected clock signal is output from the logic circuit is well known. The art is replete with references; see for example within the attached 892 column 5 lines 11-14 in Sagawa et al. (3872245) wherein clock selecting is disclosed.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to include a clock selection between an external or internal

clock being supplied to each scanning F/F with the selected clock outputted from the circuit within the AAPA as modified logic circuit wherein the selection of a clock would overcome hold-violations between the F/F circuits within the logic circuit and or allow synchronization between other circuitry using the outputted data from the last-stage F/F within the logic circuit.

5. As per claim 5, AAPA as modified teaches wherein there further comprises:

A disable-signal input terminal via which a disable signal for externally activating each scanning F/F circuit is input to the scanning controller to set an external F/F-scanning mode;

An enable output terminal via which an enable signal is output from the logic circuit, the enable signal indicating that the scanning F/F circuits are active in the sequential logical operations in the external F/F-scanning mode,

Wherein the scanning controller supplies the enable signal as an internal stall signal to the scanning F/F circuits when the enable signal is output from the logic circuit via the enable output terminal, the internal stall signal inhibiting the scanning clock signal to be supplied to the scanning F/F circuits.

Examiner notes that the disable-signal, enable signal indicating operational status, and stall signal are required when there is additional data inputted into the LFSR so that data is not lost or improper data is not added to the system. The art is replete with references; see for example within the attached 892 figure 12 and column 12 in Rajski et al. (US 6728901) wherein a LFSR is disclosed.

6. As per claim 6, AAPA as modified teaches a multiple stage F/F circuit operating as a LFSR with operation clock selections means to select between an external or internal operation clock along with means to input additional data into the multiple stage F/F circuit without data loss or improper data added to the system

AAPA as modified does not specifically teach wherein the logic circuit further comprising a parallel-to-serial converter, connected to the external scanning clock output terminal, the external scanning output terminal, and the enable output terminal, to convert parallel data output from the logic circuit to a single serial data output.

However those of ordinary skill in the art at the time the invention was made would recognize that the use of a parallel-to-serial converter to compress a number of outputs to a single output is well know. The art is replete with references; see for example patent number 3623020 on the attached 892 with this action.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to use a parallel-to-serial converter with its inputs being the external scanning clock output terminal, the external scanning output terminal, and the enable output terminal in order to compress the external scanning clock output, external scanning output, and enable output into a single output to reduce the number of outputs and subsequent connections required to obtain the output data.

7. As per claim 7, AAPA as modified teaches a multiple stage F/F circuit operating as a LFSR with operation clock selections means to select between an external or internal operation clock along with means to input additional data into the multiple stage F/F circuit without data loss or improper data added to the system.

AAPA as modified does not specifically teach wherein in response to an external rotate signal, the scanning controller advances an installed program by one cycle after one logic sequential logical operation of the scanning F/F circuit for another logical sequential operation, and in response to an external step signal, the scanning controller outputs data of the scanning F/F circuit from the logic circuit after one-cycle program advancement in response to the rotate signal and then brings the logic circuit in a halt.

However those of ordinary skill in the art at the time the invention was made would recognize that the one-cycle program advancement and output in response to a rotate signal and step signal supplied to the logic circuit wherein after the one-cycle advancement the logic circuit is halted is well known. The art is replete with references; see for example within the attached 892 column 45 lines 26-30 in Nagel et al. (4188665) wherein single cycle loading is disclosed.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to have single cycle program advancement and output in response to a rotate and step signal within AAPA as modified logic circuit to avoid bottlenecking of data wherein continues program advancement and output from the logic circuit would exceed the processing capability of circuitry using the logic circuits output.

8. As per claim 8, AAPA teaches wherein the scanning F/F circuits can be divided into a plurality of logic-circuit groups (page 2-3 lines 35-1)

AAPA as modified does not specifically teacher wherein the scanning F/F circuits are divided into a plurality of logic-circuit groups with each group including the data selector, the clock selector and the scanning controller.

However those of ordinary skill in the art at the time the invention was made would recognize that dividing the scanning F/F circuits into a plurality of logic-circuit groups with each group including the data selector, the clock selector, and the scanning controller would have been obvious since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Gegis Paper Co. v. Bemis Co., 193 USPQ 8.*

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to make this modification of dividing the scanning F/F circuits into a plurality of groups each with the data selector, clock selector, and scanning controller to implement parallel processing of data wherein the execution of parallel processing would decrease the operation and execution time of the system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100